

BUH150

SWITCHMODE™ NPN Silicon Planar Power Transistor

The BUH150 has an application specific state-of-art die designed for use in 150 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the startup conditions or under a short circuit across the load.

Features

- Improved Efficiency Due to the Low Base Drive Requirements:
High and Flat DC Current Gain h_{FE}
Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Pb-Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector-Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector-Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter-Base Voltage	V_{EBO}	10	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C I_{CM}	15 25	Adc
Base Current – Continuous – Peak (Note 1)	I_B I_{BM}	6 12	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 1.2	W W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{stg}	-65 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.85	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

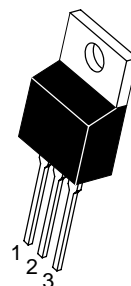
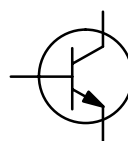
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

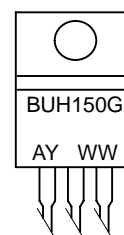
<http://onsemi.com>

**POWER TRANSISTOR
15 AMPERES
700 VOLTS, 150 WATTS**



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



BUH150 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
BUH150	TO-220	50 Units / Rail
BUH150G	TO-220 (Pb-Free)	50 Units / Rail

BUH150

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I _C = 100 mA, L = 25 mH)	V _{CEO(sus)}	400	460		Vdc
Collector–Base Breakdown Voltage (I _{CBO} = 1 mA)	V _{CB0}	700	860		Vdc
Emitter–Base Breakdown Voltage (I _{EBO} = 1 mA)	V _{EBO}	10	12.3		Vdc
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	I _{CEO}			100	μAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEs} , V _{EB} = 0)	I _{CES}	@ T _C = 25°C		100	μAdc
		@ T _C = 125°C		1000	μAdc
Collector Base Current (V _{CB} = Rated V _{CB0} , V _{EB} = 0)	I _{CB0}	@ T _C = 25°C		100	μAdc
		@ T _C = 125°C		1000	μAdc
Emitter–Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)	I _{EBO}			100	μAdc
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I _C = 10 Adc, I _B = 2 Adc)	V _{BE(sat)}		1	1.25	Vdc
Collector–Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.4 Adc)	V _{CE(sat)}	@ T _C = 25°C	0.16	0.4	Vdc
(I _C = 10 Adc, I _B = 2 Adc)		@ T _C = 125°C	0.15	0.4	Vdc
(I _C = 20 Adc, I _B = 4 Adc)		@ T _C = 25°C	0.45	1	Vdc
		@ T _C = 25°C	2	5	Vdc
DC Current Gain (I _C = 20 Adc, V _{CE} = 5 Vdc)	h _{FE}	@ T _C = 25°C	4	7	–
(I _C = 10 Adc, V _{CE} = 5 Vdc)		@ T _C = 125°C	2.5	4.5	–
(I _C = 2 Adc, V _{CE} = 1 Vdc)		@ T _C = 25°C	8	12	–
(I _C = 100 mAdc, V _{CE} = 5 Vdc)		@ T _C = 125°C	6	10	–
		@ T _C = 25°C	12	20	–
		@ T _C = 125°C	14	22	–
		@ T _C = 25°C	10	20	–
DYNAMIC SATURATION VOLTAGE					
Dynamic Saturation Voltage: Determined 3 μs after rising I _{B1} reaches 90% of final I _{B1} (see Figure 19)	I _C = 5 Adc, I _{B1} = 1 Adc V _{CC} = 300 V	@ T _C = 25°C	V _{CE(dsat)}	1.5	V
		@ T _C = 125°C		2.8	V
	I _C = 10 Adc, I _{B1} = 2 Adc V _{CC} = 300 V	@ T _C = 25°C	2.4	V	
		@ T _C = 125°C	5	V	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I _C = 1 Adc, V _{CE} = 10 Vdc, f = 1 MHz)	f _T		23		MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1 MHz)	C _{ob}		100	150	pF
Input Capacitance (V _{EB} = 8 Vdc, f = 1 MHz)	C _{ib}		1300	1750	pF

BUH150

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. $\leq 10\%$, Pulse Width = 40 μs)						
Turn-on Time	$I_C = 2 \text{ Adc}$, $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	200	300	ns
Storage Time		@ $T_C = 25^\circ\text{C}$	t_s	5.3	6.5	μs
Fall Time		@ $T_C = 25^\circ\text{C}$	t_f	240	350	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	t_{off}	5.6	7	μs
Turn-on Time	$I_C = 2 \text{ Adc}$, $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	100	200	ns
Storage Time		@ $T_C = 25^\circ\text{C}$	t_s	6.1	7.5	μs
Fall Time		@ $T_C = 25^\circ\text{C}$	t_f	320	500	ns
Turn-off Time		@ $T_C = 25^\circ\text{C}$	t_{off}	6.5	8	μs
Turn-on Time	$I_C = 5 \text{ Adc}$, $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	450	650	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	t_{off}	2.5 3.9	3	μs
Turn-on Time	$I_C = 10 \text{ Adc}$, $I_{B1} = 2 \text{ Adc}$ $I_{B2} = 2 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	500	700	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	t_{off}	2.25 2.75	2.75	μs

SWITCHING CHARACTERISTICS: Inductive Load ($V_{clamp} = 300 \text{ V}$, $V_{CC} = 15 \text{ V}$, $L = 200 \mu\text{H}$)

Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_{fi}	110	250	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	6.5 8	8	μs
Crossover Time		@ $T_C = 25^\circ\text{C}$	t_c	235 240	350	ns
Fall Time	$I_C = 2 \text{ Adc}$ $I_{B1} = 0.4 \text{ Adc}$ $I_{B2} = 0.4 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_{fi}	110	250	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	6 7.8	7.5	μs
Crossover Time		@ $T_C = 25^\circ\text{C}$	t_c	250 270	350	ns
Fall Time	$I_C = 5 \text{ Adc}$ $I_{B1} = 0.5 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_{fi}	110	150	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	3.25 4.6	3.75	μs
Crossover Time		@ $T_C = 25^\circ\text{C}$	t_c	275 450	350	ns
Fall Time	$I_C = 10 \text{ Adc}$ $I_{B1} = 2 \text{ Adc}$ $I_{B2} = 2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_{fi}	110	175	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_{si}	2.3 2.8	2.75	μs
Crossover Time		@ $T_C = 25^\circ\text{C}$	t_c	250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

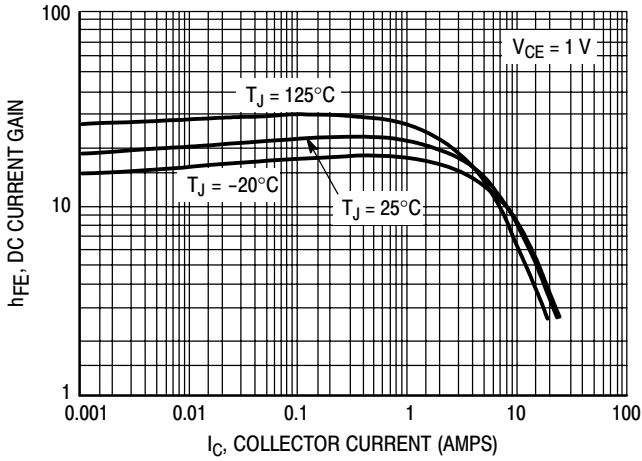


Figure 1. DC Current Gain @ 1 Volt

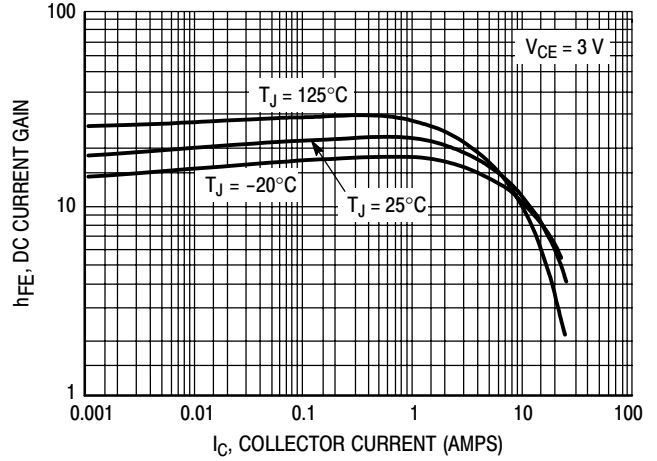


Figure 2. DC Current Gain @ 3 Volt

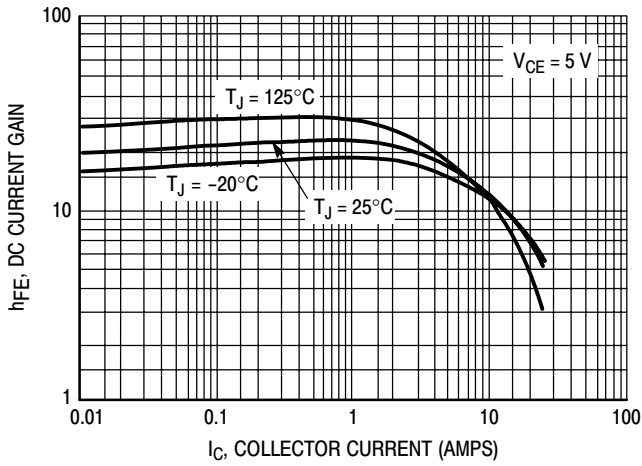


Figure 3. DC Current Gain @ 5 Volt

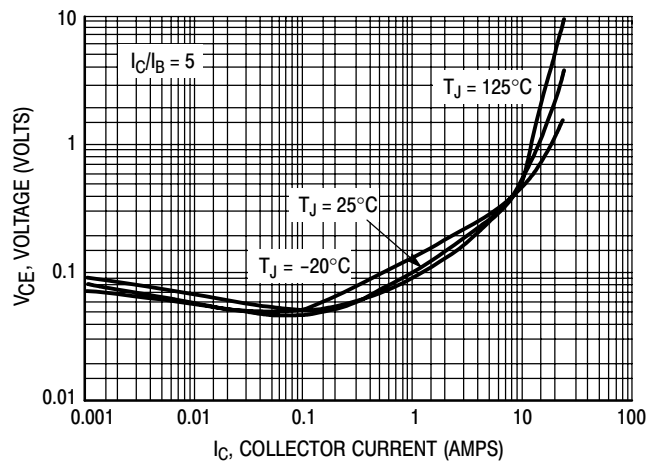


Figure 4. Collector-Emitter Saturation Voltage

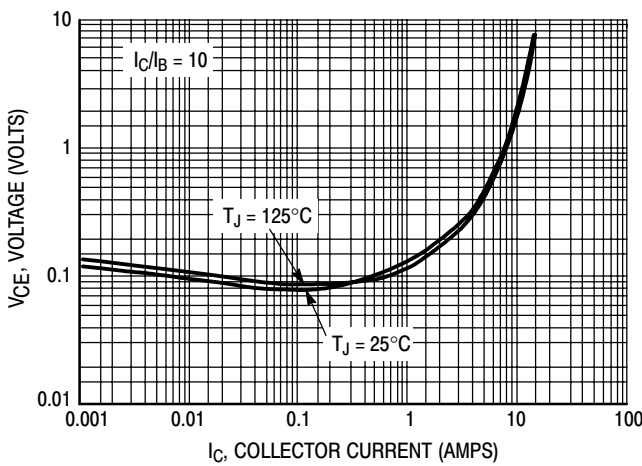


Figure 5. Collector-Emitter Saturation Voltage

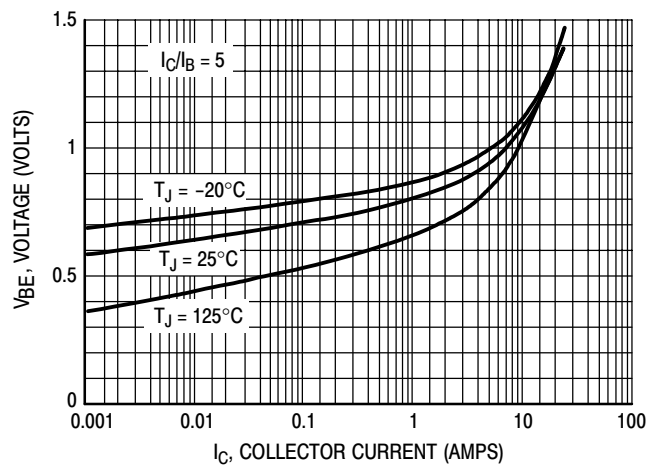


Figure 6. Base-Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

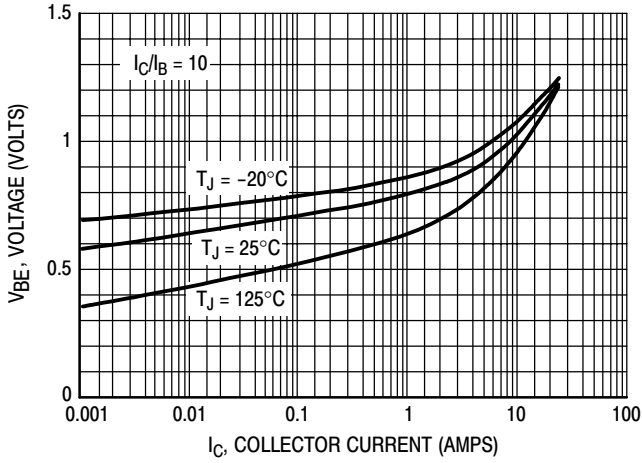


Figure 7. Base-Emitter Saturation Region

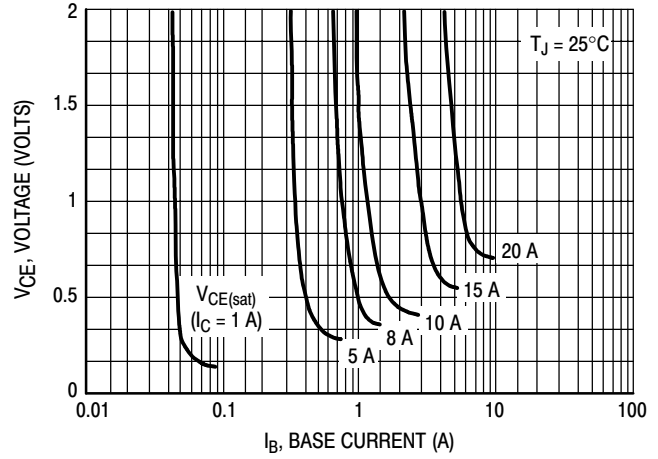


Figure 8. Collector Saturation Region

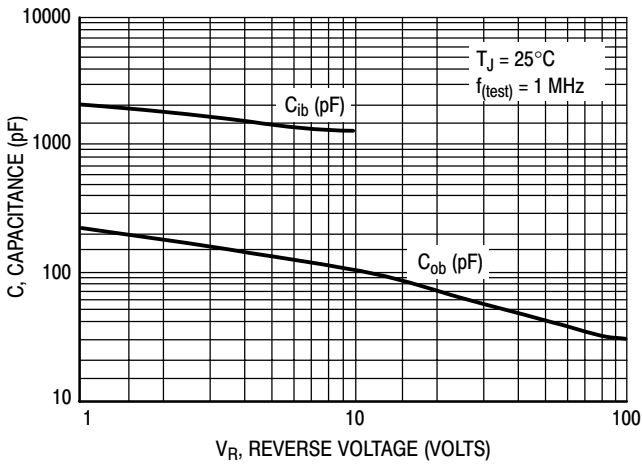


Figure 9. Capacitance

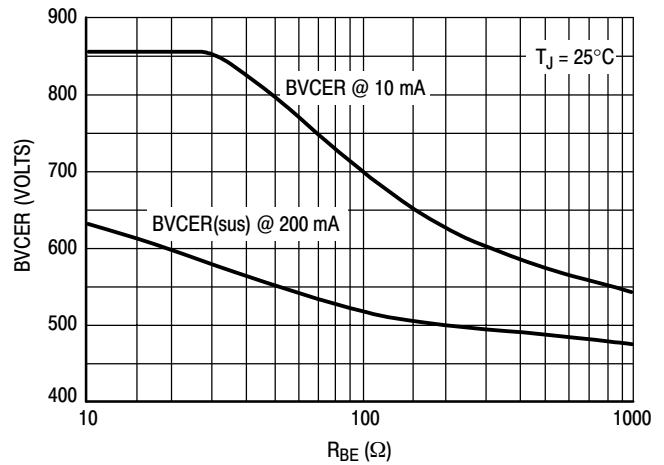


Figure 10. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

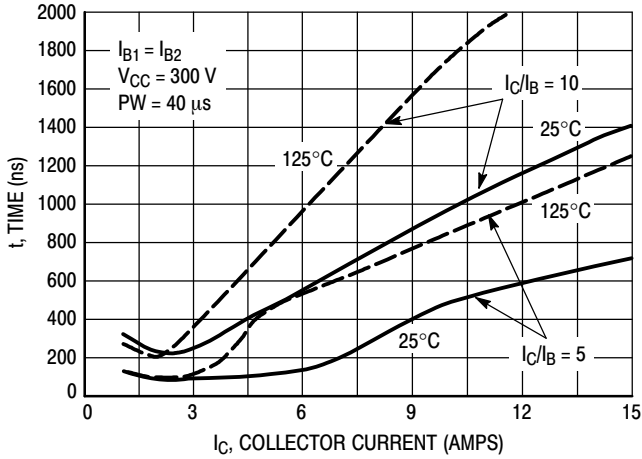


Figure 11. Resistive Switching, t_{on}

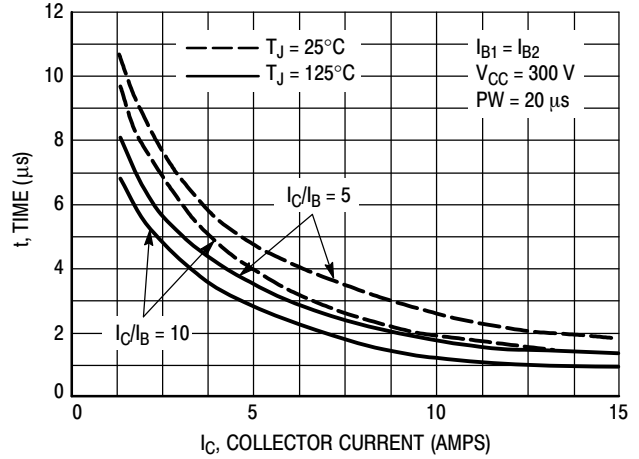


Figure 12. Resistive Switch Time, t_{off}

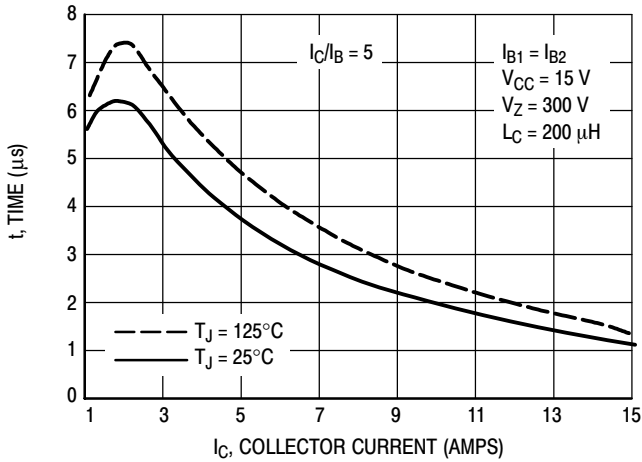


Figure 13. Inductive Storage Time, t_{si}

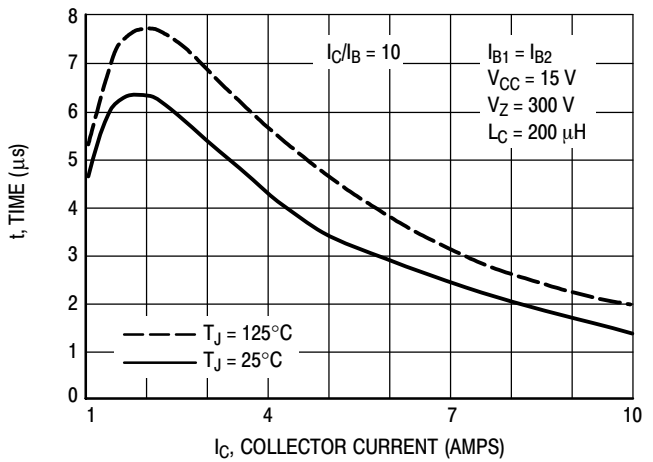


Figure 13 Bis. Inductive Storage Time, t_{si}

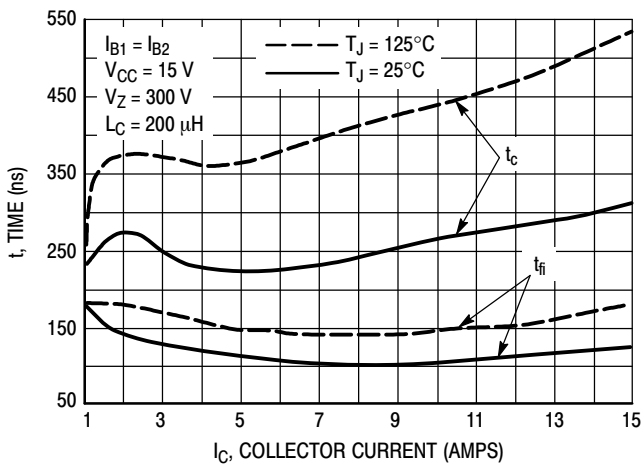


Figure 14. Inductive Storage Time, t_c & t_{fi} @ $I_C/I_B = 5$

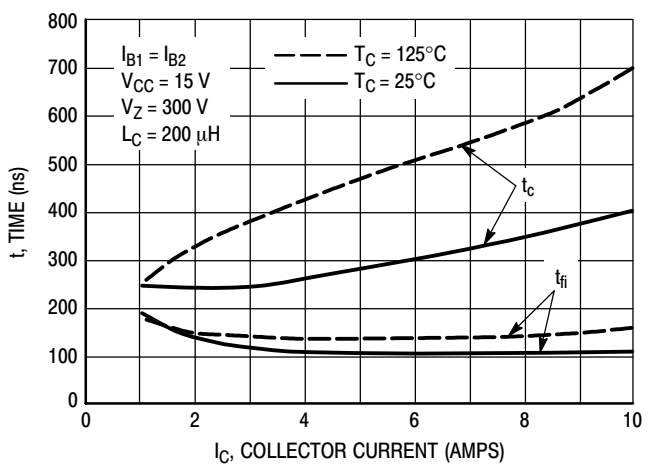


Figure 15. Inductive Storage Time, t_c & t_{fi} @ $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

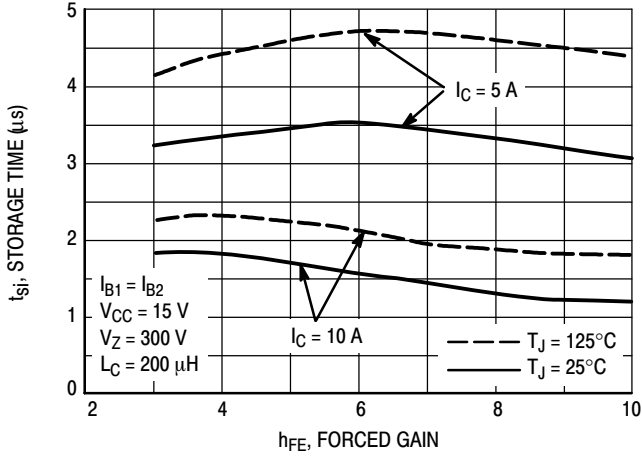


Figure 16. Inductive Storage Time

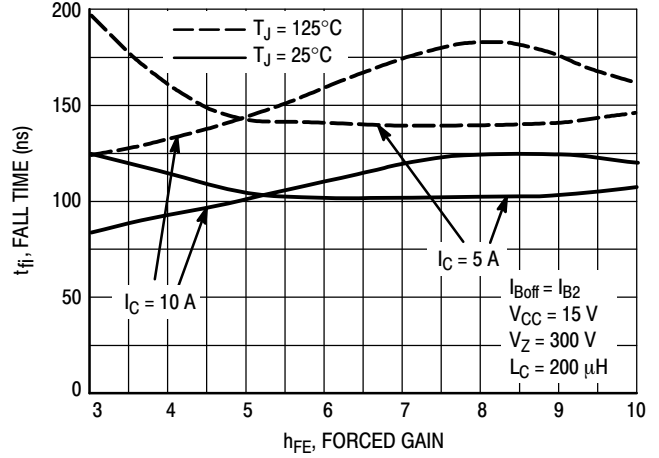


Figure 17. Inductive Fall Time

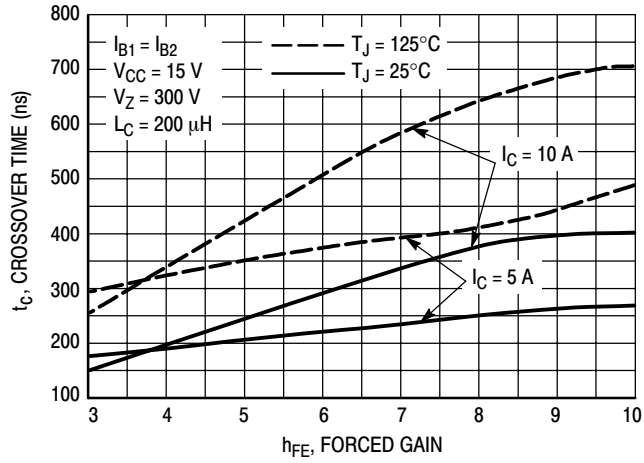


Figure 18. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

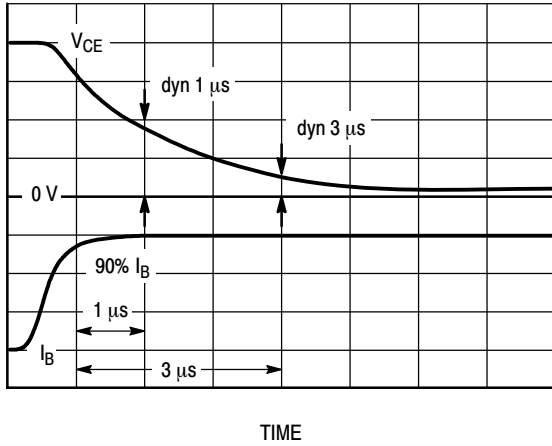


Figure 19. Dynamic Saturation Voltage Measurements

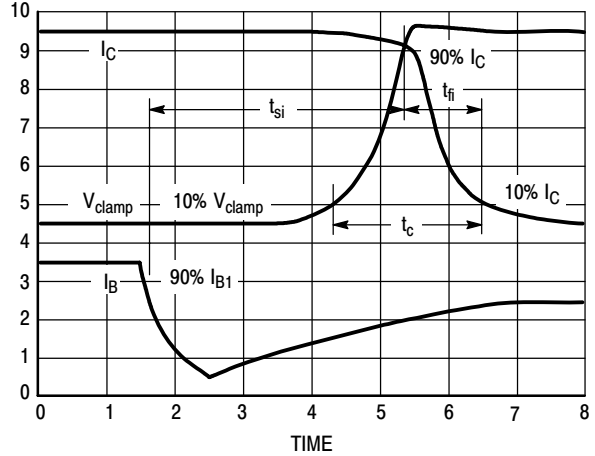
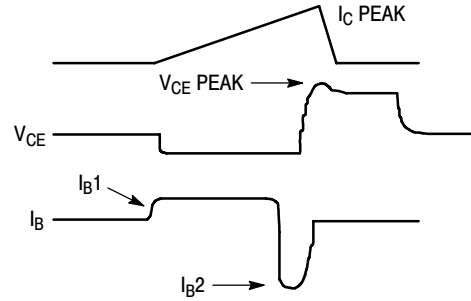
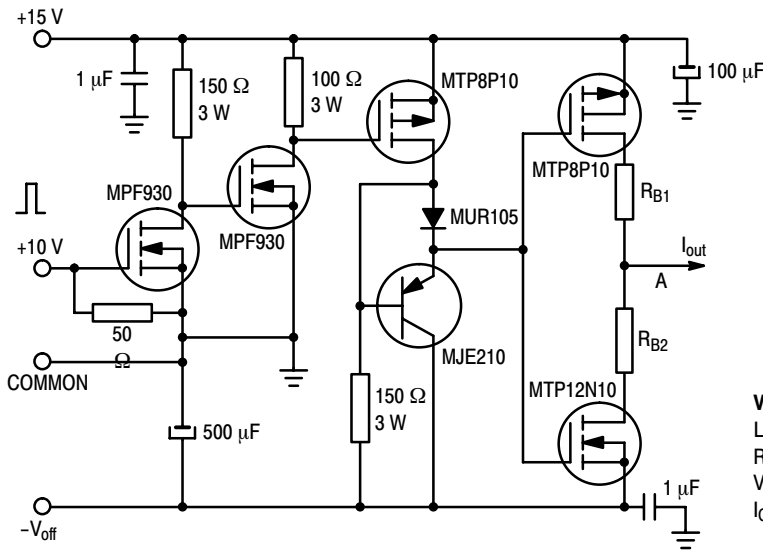


Figure 20. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$
 $L = 10 \text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20 \text{ Volts}$
 $I_{C(pk)} = 100 \text{ mA}$

Inductive Switching
 $L = 200 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 15 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 500 \mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 15 \text{ Volts}$
 R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

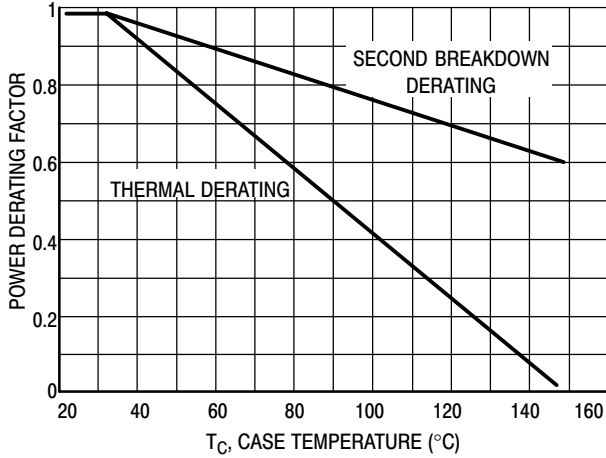


Figure 21. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

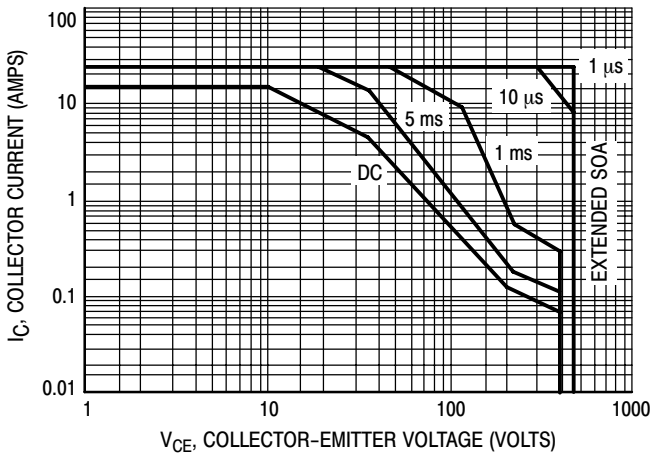


Figure 22. Forward Bias Safe Operating Area

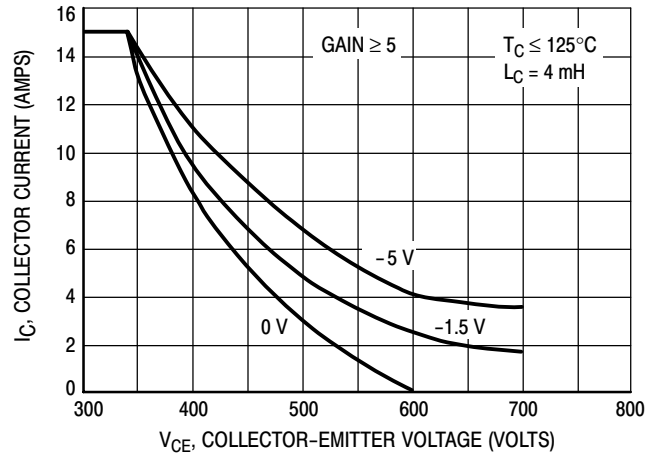


Figure 23. Reverse Bias Safe Operating Area

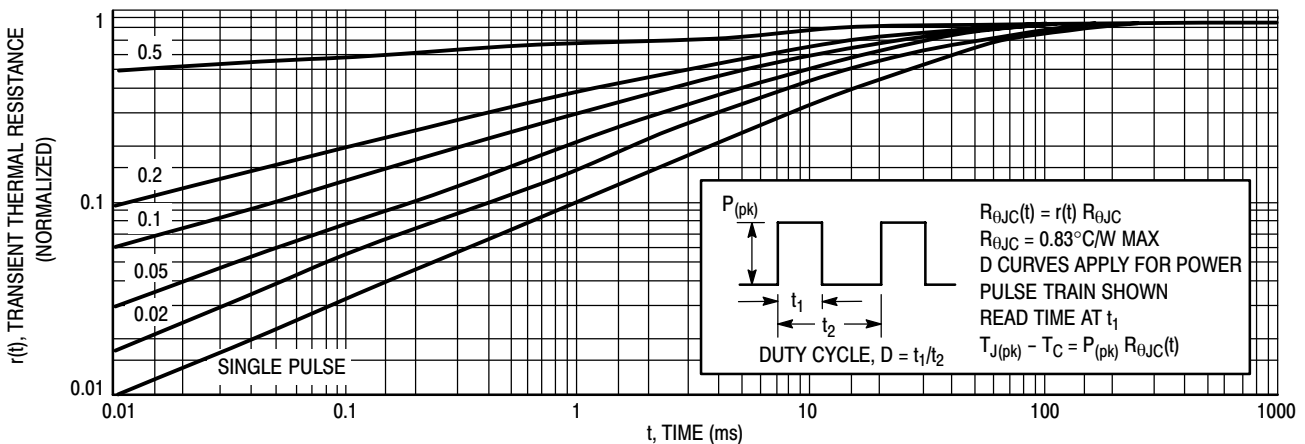
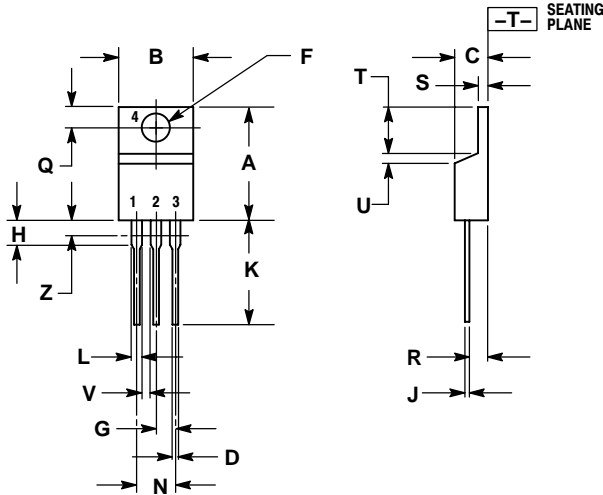


Figure 24. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH150

BUH150

PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AA



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SWITCHMODE is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.